Abstract of the Invention

Message send and receive blocks are provided to emulation ICs and reconfigurable interconnect ICs of an emulation system to reduce the multiplexed transfer latency of critical emulation signals. Each of a corresponding pair of a message send block and a message receive block is provided with a signal state value inclusion schedule to control operation of the message send and receive blocks. The signal state inclusion schedule calls for some signals within a message to be sent more often than other signals within the message. In some embodiments a parity value is implemented as part the message and included in the signal state inclusion schedule.